I claim:

1. A memory array layer for use in a 3D RRAM comprising, on a silicon substrate having peripheral circuitry thereon:

a first layer of silicon oxide, deposited and planarized;

a bottom electrode formed of a material taken from the group of materials consisting of Pt, $PtRhO_x$, $PtIrO_x$ and TiN/Pt;

a second oxide layer having a thickness of at least 1.5X that of the thickness of the bottom electrode, deposited and plainarized to a level where at the bottom electrode is exposed;

a layer of memory resistor material;

a layer of Si_3N_4;

a third oxide layer having a thickness of about 1.5X of that of the memory resistor material; CMPd to expose the memory resistor surface;

a top electrode formed of a material taken from the group of materials consisting of Pt, $PtRhO_x$, $PtIrO_x$ and TiN/Pt; and

a covering oxide layer.

2. The memory array layer of claim 1 wherein said first layer of silicon oxide has a thickness of between about 100 nm to 1000 nm; wherein said memory resistor material has a thickness of between about 20 nm to 150 nm; said Si_3N_4 layer has a thickness of between about 10 nm to 30 nm; and wherein said third oxide layer has a thickness of about 1.5X of that of the memory resistor material.

3. The memory array layer of claim 1 wherein said bottom electrode and said top electrode have, for an electrode taken from the group of electrodes formed of Pt, $PtRhO_x$, and $PtIrO_x$, a thickness of between about 50 nm to 300 nm, or for a bi-layer TiN/Pt, a thickness of between about 10nm to 200nm of TiN and between about 10 nm to 100 nm of Pt.

4. A method of programming a 3D RRAM comprising:

selecting a memory cell to be written to;

applying a high voltage programming pulse to a first related bit line;

applying a low voltage programming pulse to a second related bit line;

floating the associated word line;

Biasing all other word lines with half-programming pulse voltages; and

biasing all non-selected bit lines to the ground potential.

5. The method of claim 4 wherein reading a memory cell includes

applying a small voltage to the word lines of the non-selected bits to enhance the line voltage difference between the first related bit line and the second related bit line; and

applying a read voltage to the word line associated with the selected memory cell and detecting the voltage difference between the first related bit line and the second related bit line.

6. A method of programming a 3D RRAM comprising:

selecting a memory cell to be written to;

applying a low voltage programming pulse to a first memory resistor in the memory cell;

applying a high voltage programming pulse to a second memory resistor in the memory cell;

setting the selected word line to ground potential;

biasing all other word lines are biased to 0.5 V_P;

biasing a first related bit line with a negative programming pulse, having a pulse amplitude of $-V_P$;

biasing a second related bit line with a positive programming pulse, having amplitude of $+V_P$; and

pulsing all non-selected memory resistors with a programming voltage of between $0V_p$ and 0.5 V_p.

7. The method of claim 4 wherein reading a memory cell includes

applying a small voltage to the non-selected word lines to enhance the line voltage difference between the first related bit line and the second related bit line; and

applying a read voltage to the word line associated with the selected memory cell and detecting the voltage difference between the first related bit line and the second related bit line.